AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system, comprising:

~~a first application specific integrated circuit;~~

a first random access memory ~~coupled with the first application specific integrated circuit~~;

a first memory testing engine to execute test operations on the first random access memory;

~~a memory controller for accessing the first random access memory;~~

a first bus controller in which the first memory testing is embedded to have a memory interface which is shared with the first memory testing engine;

a processor; and

a bus to connect the processor to the first bus controller wherein the first bus controller is to provide the processor access to the first random access memory via the memory ~~controller~~interface, and the processor is to control the first memory testing engine via the bus and the first bus controller and wherein the first memory testing engine uses data, address and control pathways used by the first bus controller so that if data traffic from the processor is being passed to a memory module by the first bus controller, the first memory testing engine cannot run a test function.

2. (Currently Amended) The system of claim 1, further comprising:

~~a second application specific integrated circuit;~~

a second random access memory ~~coupled with the second application specific integrated circuit~~;

a second memory testing engine to execute test operations on the second random access memory; and

a second bus controller connected to the processor by the bus, wherein the second bus controller is to provide the processor access to the second random access memory, and the processor is to control the second memory testing engine via the bus and the second bus controller.

3. (Previously Presented) The system of claim 2, wherein the first and second memory testing engines can perform testing operations concurrently.

4. (Previously Presented) The system of claim 1, wherein the first memory testing engine is integrated with the first bus controller.

5. (Previously Presented) The system of claim 1, wherein the first memory testing engine generates test data and expected responses.

6. (Previously Presented) The system of claim 5, wherein the first memory testing engine captures and compares an actual random access memory response to the test data.

7. (Previously Presented) The system of claim 1, wherein the first memory testing engine is responsible for programmable address ranges and data widths.

8. Canceled.

9. (Previously Presented) The system of claim 1 further comprising a register controller for the processor to configure the first memory testing engine.

Claims 10-11 (Canceled).

12. (Previously Presented) The system of claim 1, wherein the first memory testing engine saves a failing address for the processor.

13. (Previously Presented) The system of claim 1, wherein the first memory testing engine saves a failing data value for the processor.

14. (Previously Presented) The system of claim 1, wherein the first memory testing engine discontinues an active test until the processor reads a failing address and a memory address location.

15. (Previously Presented) The system of claim 1, wherein the first memory testing engine reports an asynchronous interrupt to the processor.

16. (Currently Amended) A method, comprising:

transmitting a plurality of initiation signals from a processor via a bus to a plurality of memory testing engines via a plurality of bus controllers, respectively;

testing a plurality of random access memories, respectively, using the plurality of initiated memory testing engines, respectively;

accessing from the processor through the bus the plurality of random access memories via the plurality of bus controllers, respectively;

accessing from the bus controllers the random access memories using a plurality of memory controllers, respectively; and

passing control of data, address and control pathways between (1) each one of the memory test engines, and (2) a respective one of the bus controllers, so that only one of the two has control at one time.

17. Canceled.

18. (Currently Amended) The method of claim 16, ~~wherein testing by the plurality of memory testing engines is concurrent~~further comprising transmitting data traffic from the processor through the bus to one of the random access memories via the data, address and control pathways while such are under control of the respective bus controller.

19. (Original) The method of claim 16, further comprising generating test data and expected responses.

20. (Original) The method of claim 19, further comprising capturing and comparing an actual random access memory response to the test data.

21. (Previously Presented) The method of claim 16, wherein testing comprises writing multiple data patterns per memory location within a random access memory and comparing a reading of the location with an expected response.

22. Canceled.

23. (Previously presented) The method of claim 16, further comprising:

configuring the memory test engines using a plurality of register controllers, respectively.

Claims 24-25 (Canceled).

26. (Original) The method of claim 16, further comprising saving a failing address for the processor.

27. (Original) The method of claim 16, further comprising saving a failing data value for the processor.

28. (Original) The method of claim 16, further comprising discontinuing an active test until the processor reads a failing address and a memory address location.

29. (Original) The method of claim 16, further comprising reporting an asynchronous interrupt to the processor.

30. (Currently Amended) A machine-readable storage medium tangibly embodying a sequence of instructions executable by a machine to perform a method comprising:

accessing over a bus a memory associated with an application specific integrated circuit (ASIC) via a utility bus slave (UBS) controller ~~over a bus~~on the ASIC;

configuring a memory test engine (MTE) that is embedded in the UBS controller to have the same memory interface to said memory, by writing to the UBS controller over said bus; and

processing a signal from the MTE that a test of said memory is complete.

31. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed by the machine cause:

accessing a plurality of memories associated with a plurality of ASICs via a plurality of UBS controllers over the bus;

configuring a plurality of MTEs over said bus; and

processing a plurality of signals from the MTEs that tests of said memories are complete.

Claims 32-33 (Canceled).

34. (Previously Presented) The machine-readable storage medium of claim 31, further comprising instructions that when executed control the capturing and comparing of an actual random access memory response to the test data.

35. (Previously Presented) The machine-readable storage medium of claim 30, wherein the instructions are such that the testing comprises writing multiple data patterns per memory location within the memory and comparing a reading of the location with an expected response.

36. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed configure the MTE by writing to a register controller.

37. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed test memory in a decrementing memory address order.

Claims 38-39 (Canceled).

40. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed save a failing address for the processor.

41. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed save a failing data value for the processor.

42. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed discontinue an active test until a processor reads a failing address and a memory address location.

43. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed report an asynchronous interrupt to a processor.

44. (Currently Amended) An apparatus comprising:

means for ~~simultaneously testing each of a plurality of memories~~testing memory;

means for controlling a bus, the testing means being embedded in the bus controlling means to share the same memory interface;

means for initiating the testing~~; and~~ by accessing the testing means over the bus; and

means for disabling the testing means while passing data traffic from the initiating means to the memory over the bus.

~~means for giving the initiation means access to each of the plurality of memories and access to the testing means.~~

Claims 45-46 (Canceled).

47. (Original) The apparatus of claim 44, further comprising a means for generating test data and expected responses.

48. (Original) The apparatus of claim 47, further comprising a means for capturing and comparing an actual random access memory response to the test data.

Claims 49-53 (Canceled).

54. (Previously Presented) The apparatus of claim 44, further comprising a means for saving a failing address for the initiation means.

55. (Previously Presented) The apparatus of claim 44, further comprising a means for saving a failing data value for the initiation means.

56. (Previously Presented) The apparatus of claim 44, further comprising a means for discontinuing an active test until the initiation means reads a failing address and a memory address location.

57. (Previously Presented) The apparatus of claim 44, further comprising a means for reporting an asynchronous interrupt to the initiation means.